Lucas Pereira

Senior Design Verification Engineer

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Professional Summary

Verification engineer with 6+ years of experience across DSP, RISC-V, subsystem verification, and emulation.

I started in digital design and verification during my Computer Engineering journey, including FPGA-based work for hyperspectral image compression. This foundation led me to ASIC functional verification with focus on architecture, modeling, and verification quality for tapeout readiness.

I worked on DSP verification for photonics, then moved into a customer-facing emulation application engineering role at Cadence, helping customers resolve critical technical bottlenecks in complex SoC projects, including emulator/simulator interaction, debug flows, and testbench performance optimization. At Eldorado, I worked on safety-critical IP verification through final GDSII delivery and, in parallel, on RISC-V CPU verification, where I developed an in-house RISC-V Python model and contributed to international collaborations. Currently, I am a Senior Design Verification Engineer at Qualcomm, working on subsystem verification for the latest Snapdragon platforms, specifically on subsystems that contain RISC-V IP.

UVM and RISC-V Foundational Associate certified.

Professional Experience

Qualcomm Aug 2024 – Present
Senior Design Verification Engineer Cork, Ireland

- Own end-to-end RTL verification of a full subsystem block with a RISC-V processor, driving verification activities through metrics closure and sign-off.
- Contribute to verification of a larger subsystem, with focus on power and interrupt behavior, integration debug, and closure.
- Drive coverage and quality metrics through targeted tests and bug triage toward sign-off.
- Apply an AI-first approach to verification and debug, building automation scripts for daily workflows, and collaborating with architecture, design, and power teams to unblock cross-domain issues.
- Work closely with RISC-V compilation flows and toolchain.

Eldorado Research Institute Mar 2023 – Aug 2024
Digital IC Verification Engineer Campinas, Brazil

- Developed CPU verification plans and UVM testbenches.
- Implemented Python reference models.
- Worked daily with Verilog/SystemVerilog, DPI-Python integration, and UVM.
- Executed verification beyond RTL, including GLS, timing analysis, and power analysis.
- Worked on safety-critical IP verification through final GDSII delivery.
- Worked closely with RISC-V compilation flows and toolchain.

Cadence Design Systems Mar 2022 – Mar 2023
Senior Application Engineer Remote

- Worked as a customer-facing emulation specialist, providing technical support for complex SoC verification flows.
- Diagnosed and resolved issues across emulation/simulation interaction, debug flows, and testbench adaptation for customer environments.
- Worked hands-on with emulator platforms, performance evaluation, and testbench optimization to improve runtime and verification efficiency.

- Contributed to internal technical projects to improve tooling usage, deployment practices, and engineering productivity.

Eldorado Research Institute Mar 2020 – Mar 2022
Digital IC Verification Engineer Campinas, Brazil

- Verified high-speed ASIC DSP blocks.
- Drove verification planning and reference model implementation.
- Developed scripting and UVM-based verification flows.
- Supported GLS execution, timing analysis, and power analysis.

Education

Computer Engineering 2014 – 2018
University of Vale do Itajai Itajai, SC, Brazil

- As a course completion work, I implemented in Xilinx FPGA an accelerator for the prediction step of the CCSDS 123 standard for compression of hyperspectral images.
- This project led to a publication at ISCAS 2019.

CI Brasil Apr 2019 – Feb 2020
Universidade de São Paulo São Paulo, SP, Brazil

- National training program funded by the Brazilian federal government, focused on integrated circuit design education.

Technical Skills

Verification: UVM/UVM-A, testbench architecture, verification planning, testbench acceleration
RTL & Modeling: SystemVerilog/Verilog, Python and C/C++, scripting
Emulation: emulation/simulation co-debug, testbench adaptation, performance analysis
Domain: RISC-V, computer architecture, interrupt/power-focused subsystem verification
Tools & Environment: Linux, versioning tools

Certifications

- RISC-V Foundational Associate (Credly)
- UVM Certified (Credly)

Publications

- A low-cost hardware accelerator for CCSDS 123 predictor in FPGA (ISCAS 2019)
- Analysis of LEON3 systems integration for a Network-on-Chip (LATS 2018)